Key Processes for Fabrication of the MIT Microengine

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ABSTRACT

These lecture notes address issues of the processes required to fabricate the MIT microengine. Three key process steps are examined: Deep reactive ion etching, silicon direct wafer bonding and the fabrication process chain for Si/SiC hybrid structures. A design of experiments approach was taken to characterize the deep reactive ion etching process. A mechanics framework was established for wafer bonding. Key factors in the fabrication of Si/SiC hybrid structures have been identified as: deposition of low residual stress SiC, planarization by polishing processes, and use of a SiO_2 interlayer to permit bonding.

1.0 INTRODUCTION

This lecture provides an overview of the key process steps pertinent to the MIT microengine. A schematic cross-section of the microengine is shown in figure 1. The major structural and fluidic components of the engine are created by highly anisotropic deep reactive ion etching combined with wafer bonding to create closed fluid channels. The bond lines are clearly apparent in figure 1. The device consists of six wafers, of particular concern the turbine/compressor rotor consists of two bonded wafers. Future generations of the device will utilize Si/SiC hybrid structures as described in the first lecture of this series. Each of these process steps will be examined in turn in the course of this lecture.

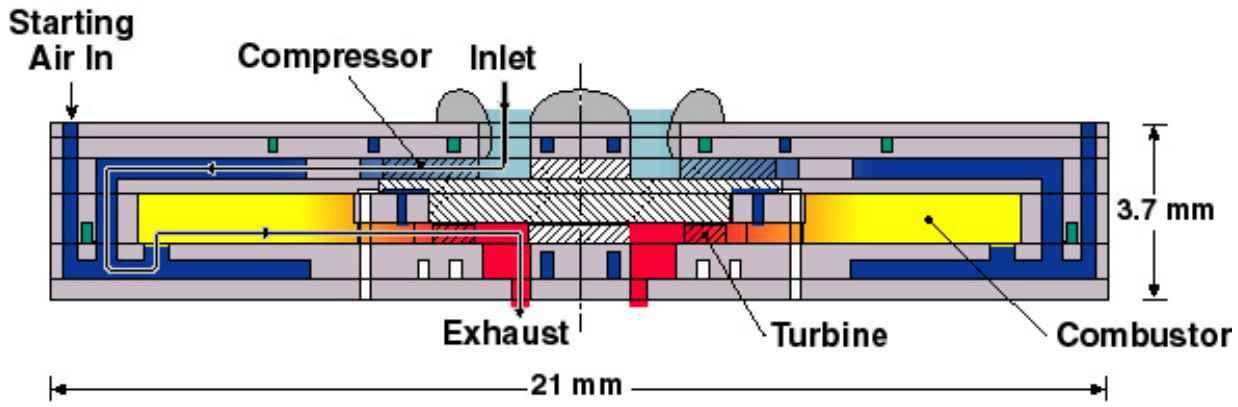


Figure 1: Cross-Sectional Schematic of MIT Microengine.

Spearing, S.M. (2005) Key Processes for Fabrication of the MIT Microengine. In *Micro Gas Turbines* (pp. 9-1 – 9-18). Educational Notes RTO-EN-AVT-131, Paper 9. Neuilly-sur-Seine, France: RTO. Available from: http://www.rto.nato.int/abstracts.asp.

2.0 DEEP REACTIVE ION ETCHING (DRIE)

The MIT microengine project makes heavy use of the deep reactive ion etching process originally developed and patented by the Bosch company. This process allows very high aspect ratio microstructures with very vertical sidewalls. The MIT microengine structures are fabricated using etching tools produced commercially by STS. The DRIE process achieves high aspect ratios and vertical sidewalls by using a repeated two stage (time multiplexed) etching cycle. This is shown schematically in figure 2 and Figure 3. In the first stage a SF_6 plasma etch is conducted, in the second C_4F_8 is deposited over the entire wafer. This process is repeated throughout the etching process. The directionality of the plasma etch breaks through the deposited C_4F_8 on the horizontal surfaces, but leaves the C_4F_8 on the side walls. When properly tuned the process can result in very vertical side walls albeit with micro-scale scalloping from the cyclic nature of the etch, as shown in figure 4. The process can create features hundreds of microns deep, although diffusional processes for the transport of the etch/passivation gases and for the removal of the etch reaction products limits the achievable aspect ratio of trench etches to the order of 30-40:1. Masking for deep etches typically consists of a combined silicon oxide or nitride hard mask in combination with a standard polymer photoresist.

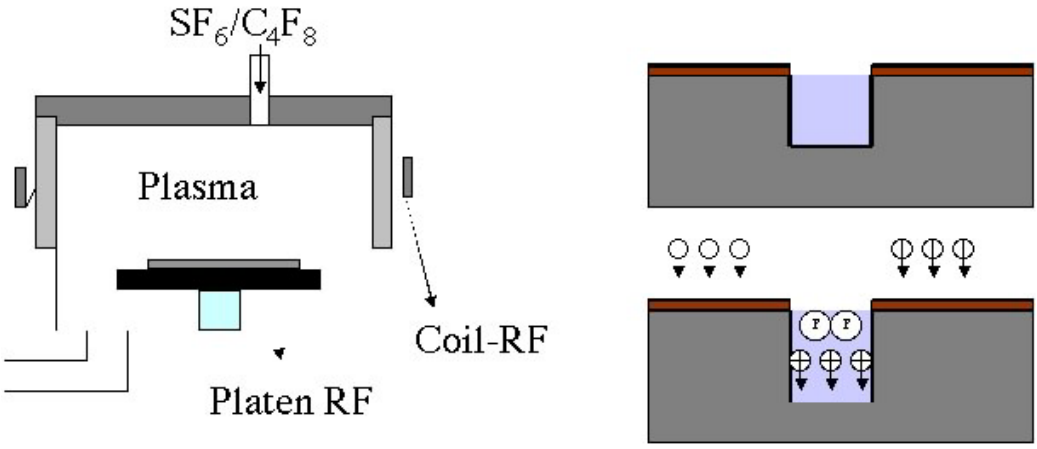


Figure 2: Schematic of Time Multiplexed Deep Reactive Ion Etching.

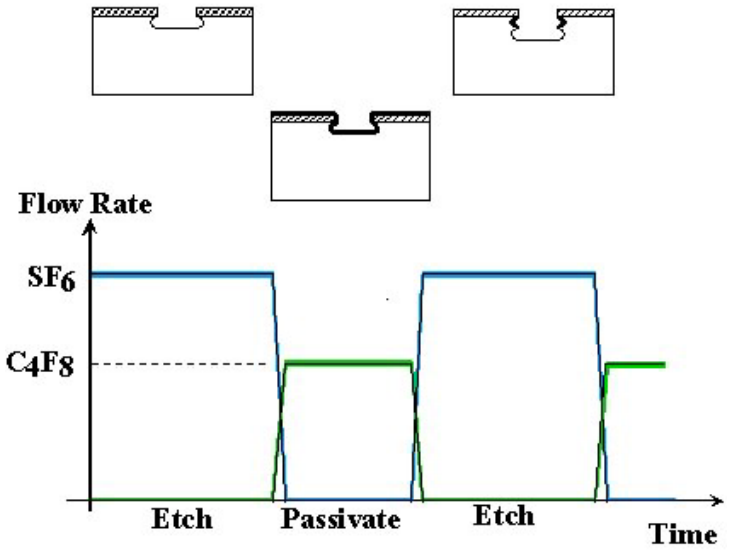


Figure 3: Schematic of Etch/Passivation Cycle of TMDE and Resulting Etch Characteristics.

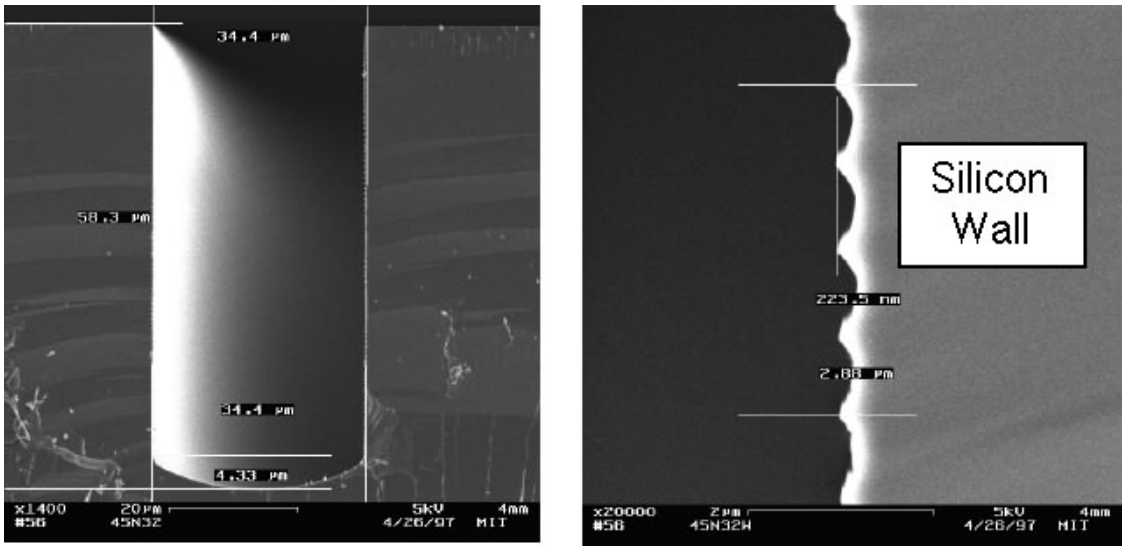


Figure 4: Cross-Sectional Micrographs of Vertical Side Walls from TMDE of Silicon.

The most critical etched dimensional tolerance of the microengine are the journal bearings. These are located on the circumference of the compressor and turbine. They are air bearings. They require very parallel sided etch walls, to avoid generating an axial load component. The bearing gap, as etched must be on the order of 10 – 15µm in width. The bearing length (etch depth) must be greater than 300 µm, and deeper etches are desirable. The bearing width must be controlled to better than 1 µm along the bearing length. These requirements motivated an extensive study of the etch characteristics with a view to identifying etch "recipes" that meet the desired bearing dimensional tolerances while maximizing the etch rate. A "design of experiments" approach was adopted, in which key process variables were identified and response surfaces conducted. This series of experiments are described in detail elsewhere [1]. Key process variables explored include:

1) In the etching cycle: SF_6 Flow Rate, Electrode Power, Etching Cycle Duration, Cycle Overlap, Coil Power;
2) In the passivation cycle: Electrode Power, C_4F_8 Flow Rate, Passivating Cycle Duration, Cycle Overlap, Coil Power; and
3) The chamber pressure (as controlled by the APC control valve).

These were varied in a series of 4 and 8 parameter experiments. Trench structures of varying widths were used to characterize the etches, as shown in figure 5. From measurements on such structures response surfaces, such as the example shown in figure 6. Similar response surfaces were conducted for other key variables, such as aspect ratio, parallelism, loading effects and the effect of etching on strength [2]. An additional key parameter is the uniformity of the etch depth across a wafer. This important in order to maximize the yield achieved from wafer level processing. Figure 7 shows an etch uniformity map across a wafer. These experiments and the resulting empirical models have been very influential in guiding the development of processes that can meet the goals of them microengine project. There is considerable scope for developing more physically-based models for the deep etching process, and it is anticipated that this will become critical as TMDE starts to be used for the mass production of devices.

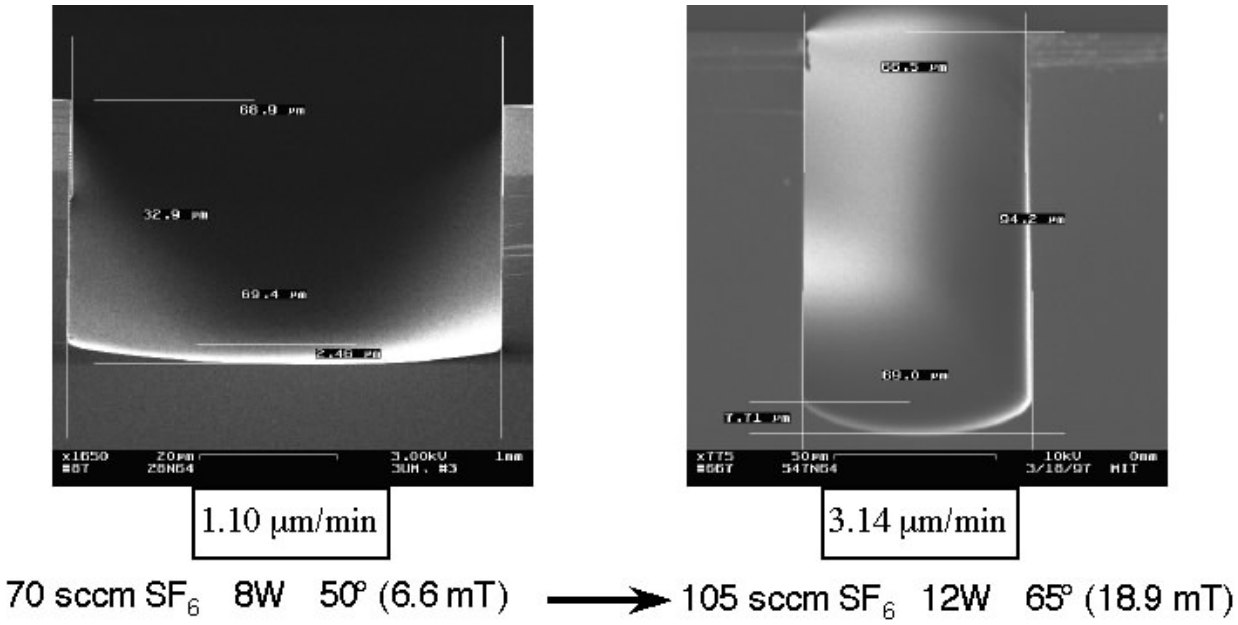


Figure 5: Examples of Trench Structures Etched at Two Different Process Conditions.

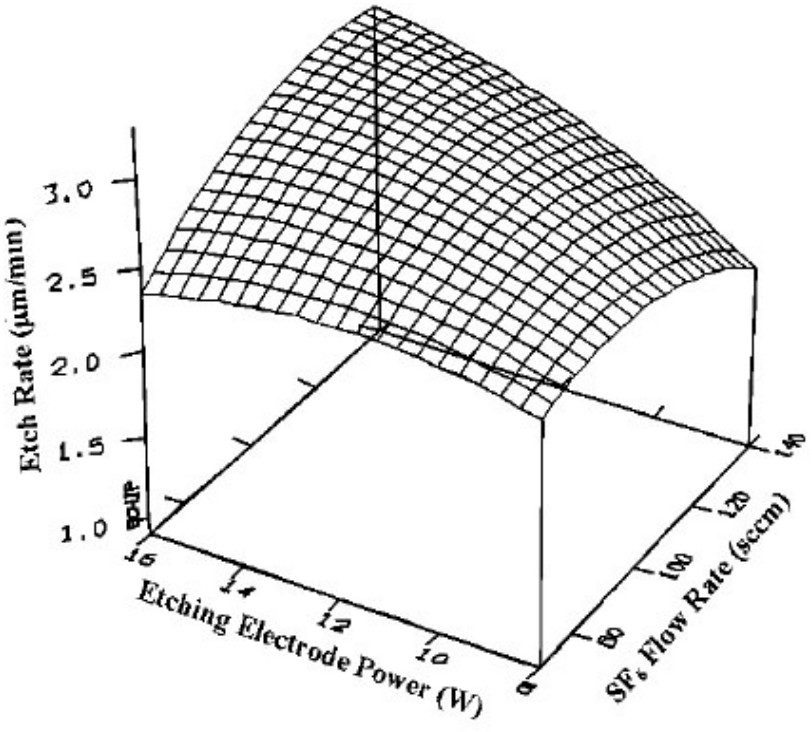


Figure 6: Examples of a Response Surface for the Deep Reactive Ion Etching Process, Plotting Etch Rate as a Function of Electrode Power and SF6 Flow Rate.

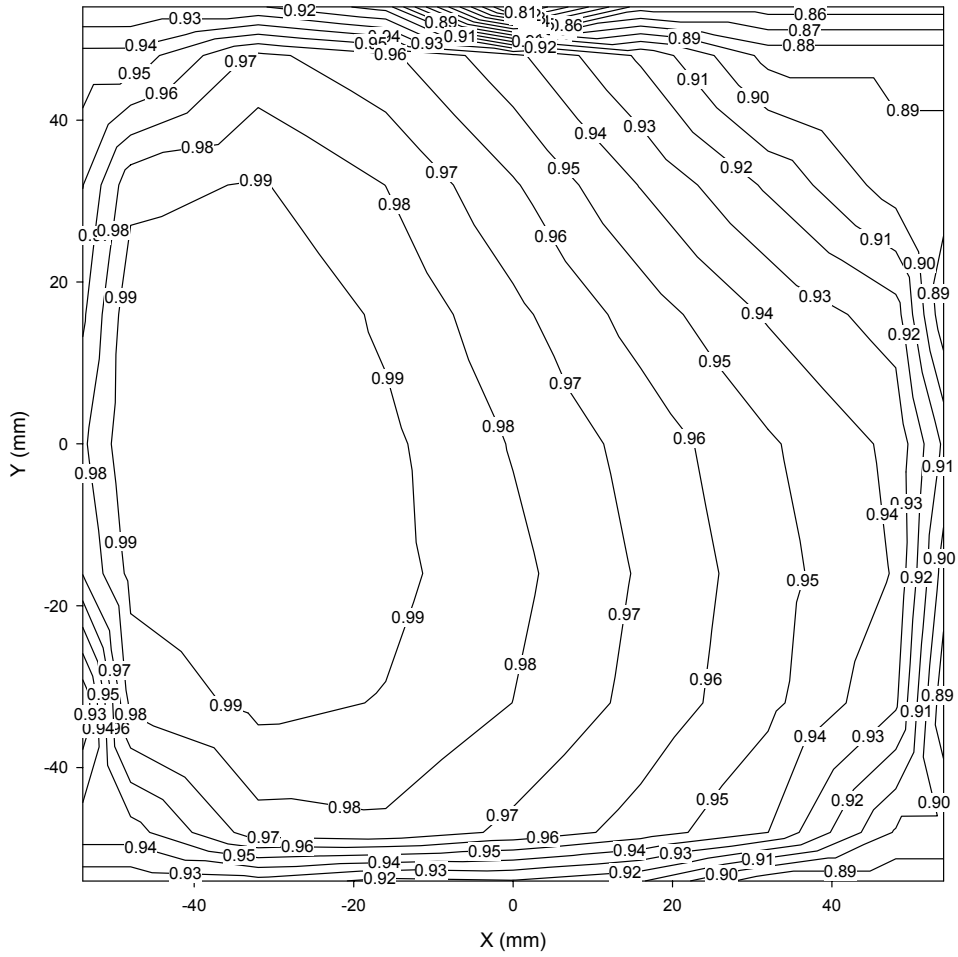


Figure 7: Etch Depth Uniformity Map across a Wafer. Note the map is for a square region 100 mm x 100 mm, and is an artefact of the software used to construct the contours. The contours are normalized to the deepest etch depth achieved on the wafer.

3.0 WAFER BONDING

The three dimensional structure of the microengine shown in figure 1 is highly dependent on the bonding of multi-wafer stacks. A cross-section of a turbine rotor test rig is shown in figure 8. Since bonding is used towards the end of the fabrication process chain, after the wafers have been etched individually, it is critical that high process yields are achieved. The preferred process was silicon direct wafer bonding. In this process there are three key steps:

1) Cleaning and surface preparation of the wafers;
2) A room temperature contacting step, resulting in a low strength bond, but with intimate contact between the wafer surfaces; and
3) A high temperature (typically >1000°C) annealing step, resulting in a bond strength equal to that of monolithic silicon.

Although there are issues associated with all three steps, in the context of the microengine project, the contacting step (2) was found to be the most crucial. A comprehensive review of wafer bonding technology can be found elsewhere [3].

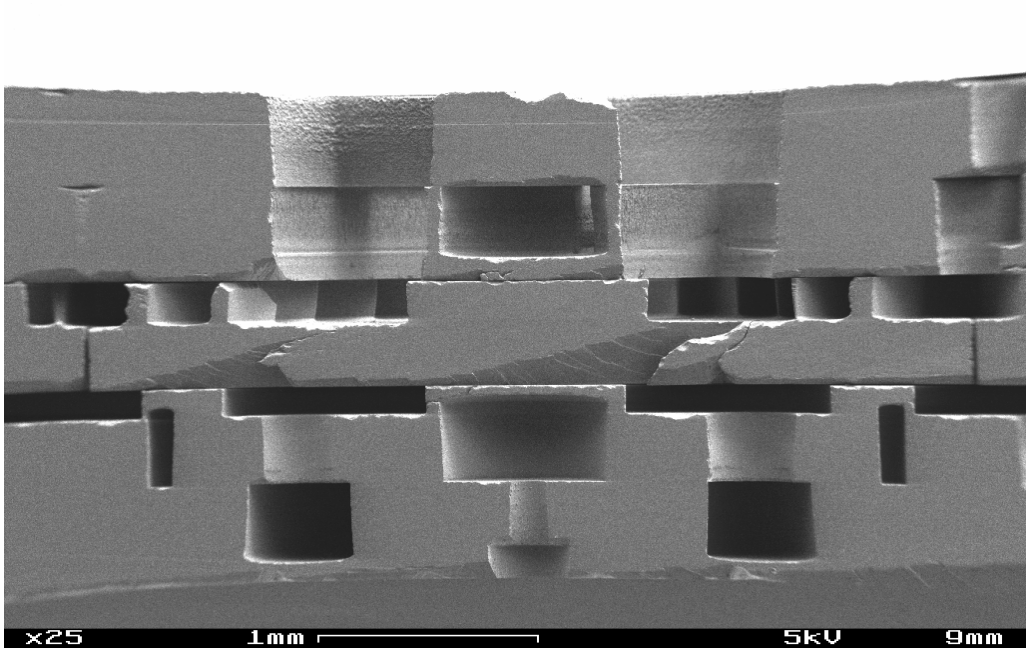


Figure 8: Cross-Section of a Micro-Bearing Rig showing Five Wafer Bonded Layers. The rotor rotates at up to 1.35 million RPM.

3.1 Contacting Step

Contacting proceeds at room temperature. Commercial tooling is available for the alignment and bonding process. The equipment used for the microengine fabrication is an EVG 501 aligner/bonder system. The wafer pairs (or stacks) to be contacted are aligned, using optical alignment marks, derived from those used for lithographic mask alignment. The aligned wafer pair are then pressed together at their centres, and the bond front progresses outward. This is shown in figure 9.

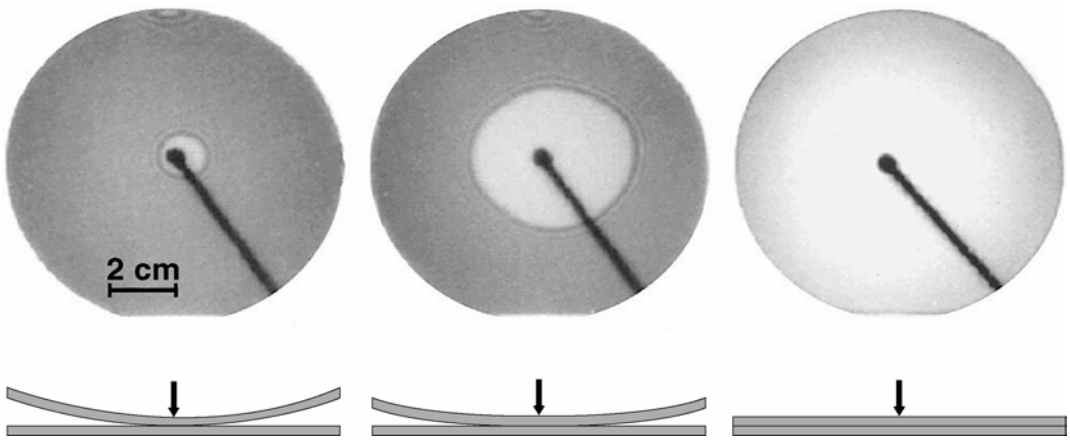
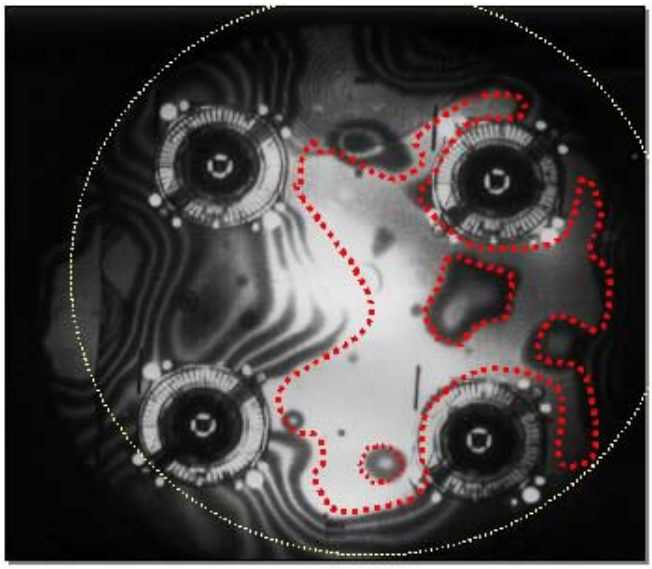


Figure 9: Infrared Images of Bond Front Progression from a Pair of Silicon Wafers (from ref. [3]).

The ability to inspect contacted wafers in the near infrared is very useful as it allows determination of whether a good bond has been achieved. If there are visible defects are observed the wafer pair can be separated, recleaned, and the contacting process can be retried. Once the high temperature annealing step is taken, no rework can be achieved.

Figure 10 shows a wafer stack from a microengine build. The interference fringes show clearly that the bond interfaces are not well bonded. In order to understand the key elements of the contacting process, a comprehensive study was undertaken. This is documented fully elsewhere [4, 5, 6, 7, 8, 9].



(photo courtesy MIT Microengine - N. Miki)

Figure 10: Infrared Image of a Microengine Wafer, Showing no Well Bonded Engine Dies.

At the heart of the room temperature contacting step is the formation of secondary (weak) intermolecular bonds between adsorbed species on the wafer surfaces. These are hydrogen bonds between surface observed water molecules, as shown schematically in figure 11.

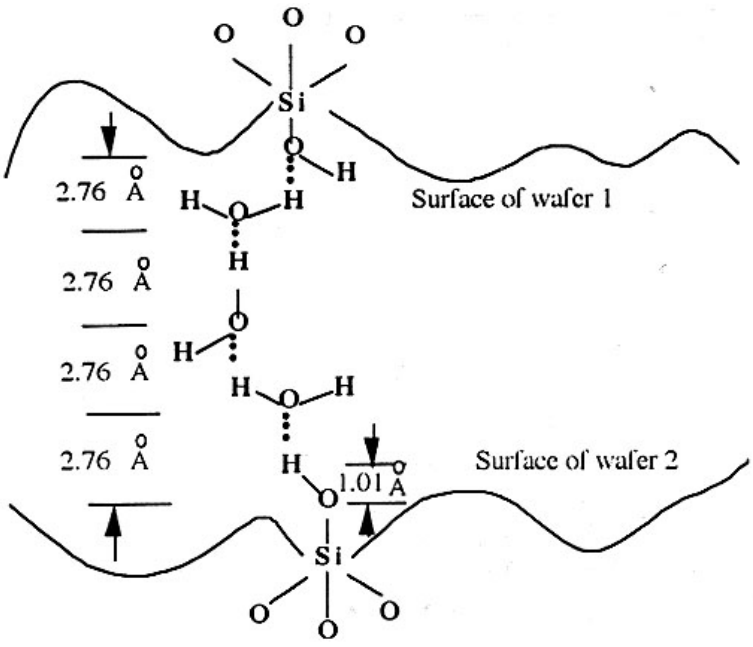


Figure 11: Schematic of Hydrogen Bonded Water Molecules between Wafer Surfaces [3].

The effect of these weak-intermolecular interactions can be quantified as a surface energy. In this way the bonding process can be thought of as a competition between the surface energy (or interface energy for a bonded pair of wafers) due to the wafer surface chemistry, and the mechanical strain energy associated with deforming the wafers to a common shape. This is shown schematically in figure 12.

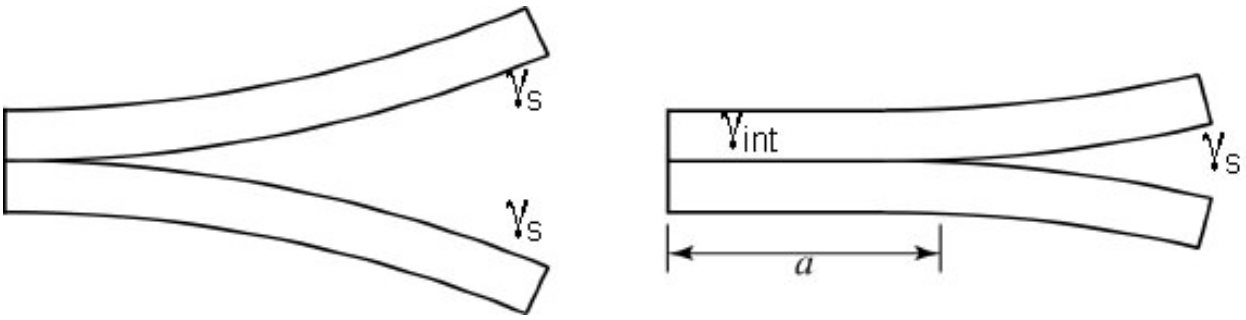


Figure 12: Schematic of the Competition between Surface Energy and Wafer Deformation.

The surface chemsitrycontributions (surface and interfacial) can be combined as a single quantity, the work of adhesion, W, as shown schematically in figure 13. Similarly the various contributions to the stored elastic strain energy can be combined as a single quantity, U_E.

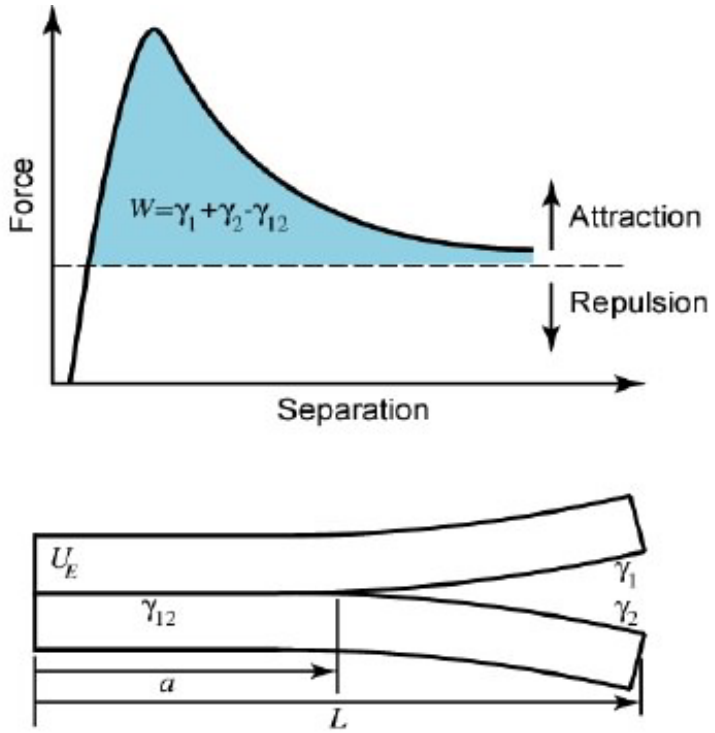


Figure 13: Schematic of the Contributions to the Work of Adhesion, W.

The criterion for bond front propagation then becomes:

$$\frac{dU_E}{dA} \leq W \qquad (1)$$

where dU_E/dA is the strain energy accumulation rate, or the elastic strain energy accumulated per unit area of bond created. This formalism allows assessment of the relative importance of the factors which might affect the bond quality achieved during contacting. Factors of particular concern to the microengine projected are: effect of wafer bow, effect of nanotopography (from chemo-mechanical polishing), effect of surface roughness, effect of particles, effect of wafer stacking sequence, effect of tool compliance and the effects of patterning. These are shown schematically in figure 14.

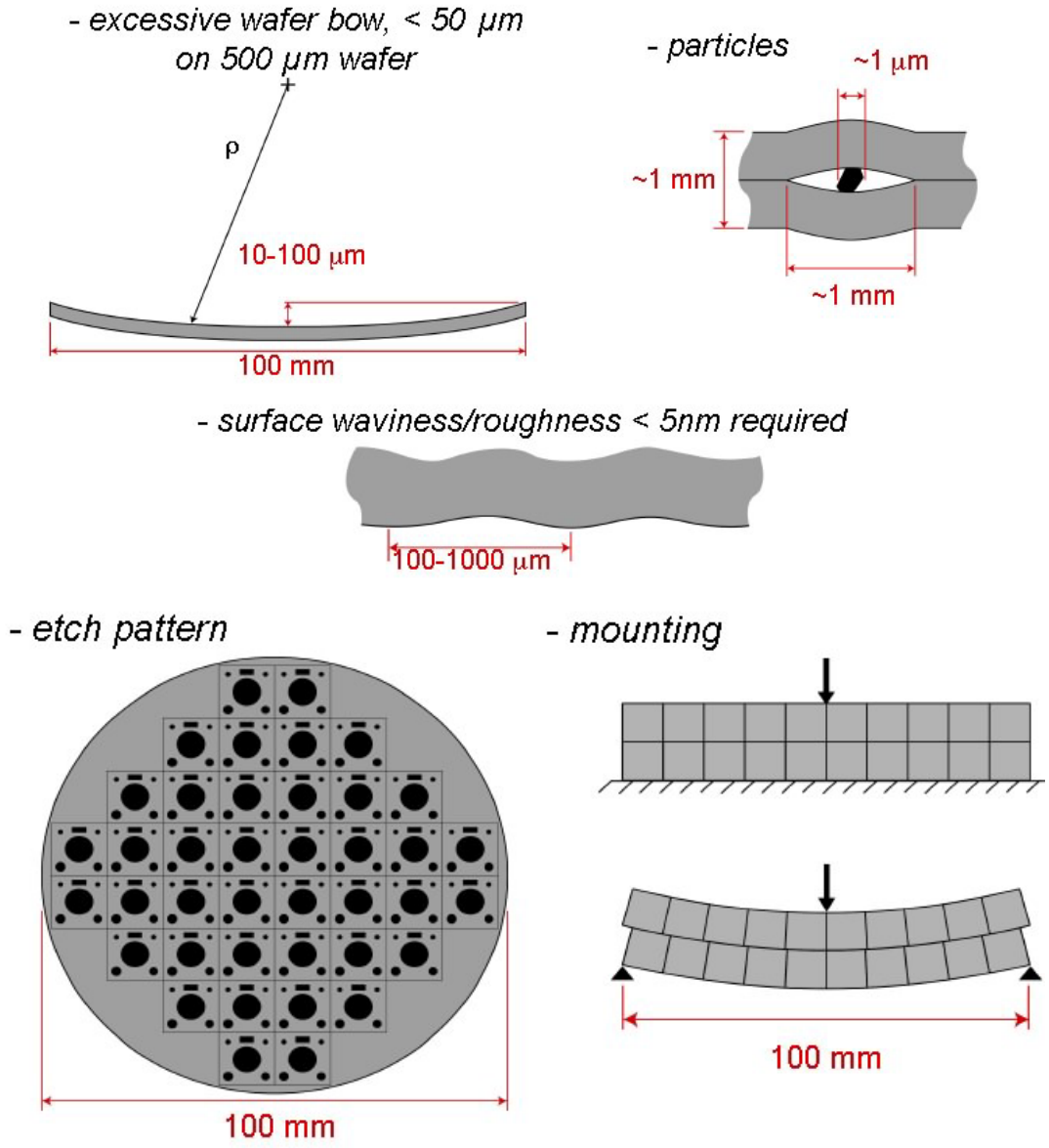


Figure 14: Schematic of Sources of Bond Quality Variation Investigated.

3.2 Effect of Wafer Bow

Insight regarding the influence of initial wafer shape (bow) can be achieved by using equation (1) in conjunction with classical plate mechanics [4]. For a pair of equal thickness circular plates, with initial curvatures, κ_o, achieving final curvatures, κ_f, the strain energy accumulation rate can be expressed as a function of relative bond front position, R, (normalized to the outer radius of the wafers) as:

$$\frac{dU_T}{dA} = \frac{1}{6}Eh^3(\kappa_f - \kappa_o)^2\frac{(1+\nu)}{(1-\nu)}\frac{1}{\left[(1+\nu)+R^2(1-\nu)\right]^2} \quad (2)$$

E and ν are the Young's modulus and Poisson's ratios of the wafers, h is the wafer thickness. The key features of equation (2) are the cubic dependence on wafer thickness, the quadratic dependence on initial curvature and the inverse quadratic dependence on bond front position. These trends are shown in figure 15 for typical wafer thicknesses and diameters.

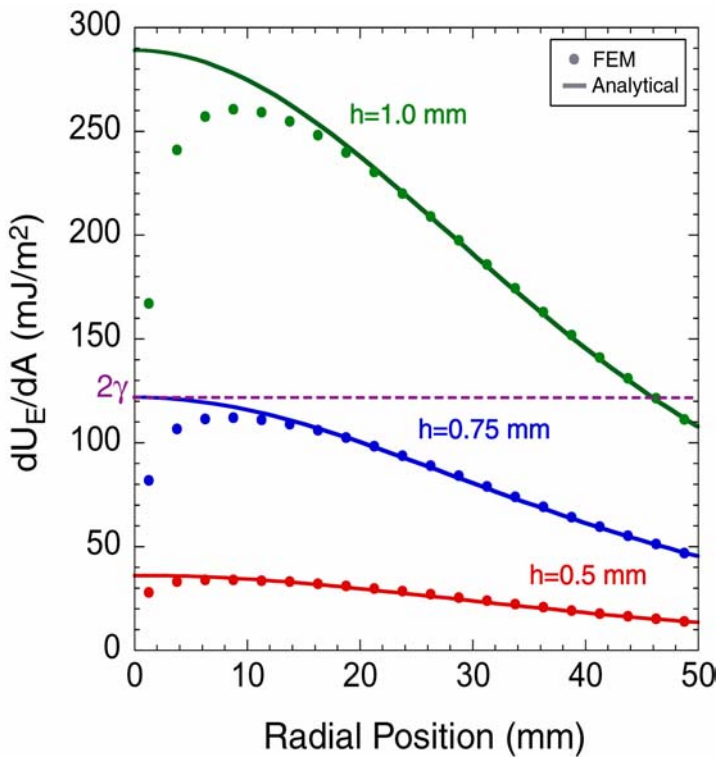


Figure 15: Calculations of Strain Energy Accumulation Rate vs. Bond Front Position, for Three Wafer Thicknesses.

The doubling of wafer thickness from 0.5 mm to 1.0 mm introduces a factor of eight increase in the resistance to bonding and the inverse dependence on bond front position implies that bonding becomes easier as the bond front moves towards the outer radius. An effect which is borne out by experiments on blank wafers. The strong dependence on wafer thickness has serious implications for the ability to bond multi-wafer stacks. In particular it is vital that in bonding stacks an incremental approach is used, in which individual wafers are added to existing stacks, rather than by creating two sub-stacks of equal thickness and then attempt to bond them together to create the full stack.

3.3 Effect of Patterning

There are two principal effects of patterning wafers: (1) for shallow etching, bonding area is removed, which reduces the effective work of adhesion available to propagate the bond front. (2) for deep etching, material is removed from the bulk of the wafer, which will reduce the effective stiffness of the wafers. These can be explored using the mechanics framework described above.

3.3.1 Shallow Etching

This effect can be analyzed simply by considering the problem of radial spoke patterns, which either broaden or taper with radial position, according to a linear function. Sample patterns are shown in figure 16. A modified version of equation 2 results, with a linear variation of area with radius.

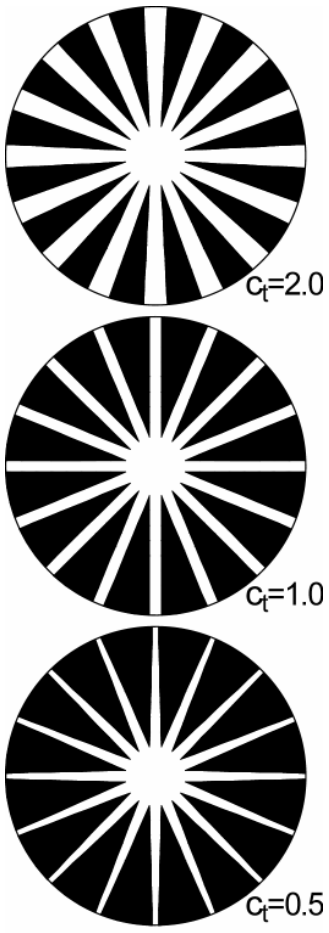


Figure 16: Tapered Spoke Patterns, dark areas are shallow etched.

For different taper ratios the curves shown in figure 17 result. Key features, are that for a tapering spoke patterns the strain energy accumulation rate increases with bond front position. Implying that bonding becomes more difficult as the bond front moves out radially.

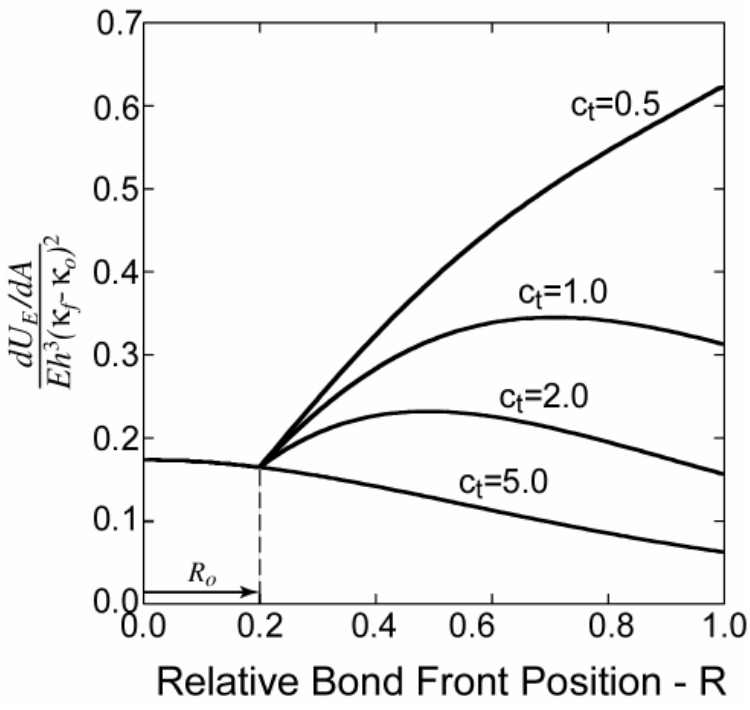


Figure 17: Strain Energy Accumulation Rate vs. Bond Front Position for Radial Spoke Patterns.

3.3.2 Deep Etched Patterns

This effect can be analyzed by considering deep etching to create porous material throughout the wafer, according to some volume fraction, c_E. This then permits the use of a porous material model to calculate the effective Young's modulus of the etched wafer. This is shown schematically in figure 18.

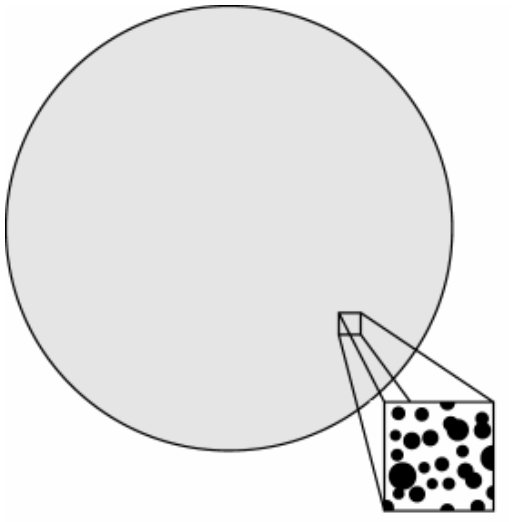


Figure 18: Schematic of a Porous Etched Wafer.

Again a modified version of figure 2 can be employed. Two particular cases are considered. One in which a shallow etch resulting in porosity is applied only to the wafer surface and a second in which bulk material is removed, which results in a reduction in stiffness. These results are plotted in figure 19.

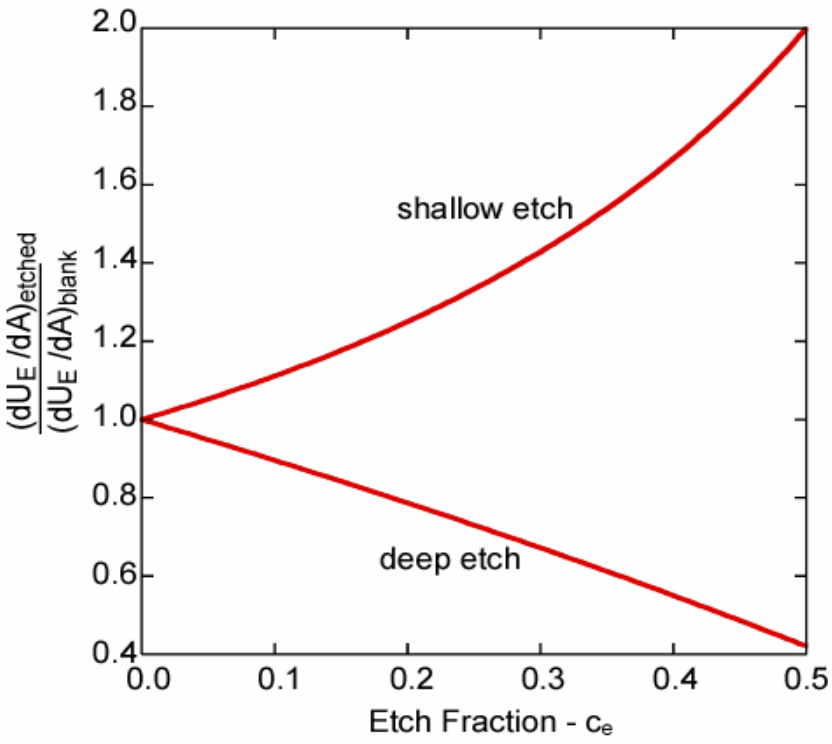


Figure 19: Strain Energy Accumulation Rate vs. Etched Volume Fraction for Deep and Shallow Etches.

As in figure 17, it is clear that a shallow etch results in an increasing resistance to bonding, however, a deep etch can reduce the resistance to bonding. This is due to the dominance of the reduction in stiffness over the reduction in bondable area. This suggests that patterning, for deep etched devices such as the microengine is unlikely to be a particular detriment to bondability. However, detailed analysis of particular patterns is probably required.

3.4 Other Factors on Bonding

Other analysis and associated experiments have revealed that the major source of bond failures on the microengine project was the accumulation of wafer bow in forming multiple wafer stacks. As noted in section 3.2, thick stacks with significant bow are very difficult to bond. This problem is worsened by the use of compliant tooling, particularly polymer coated chucks during the contacting process. This allows pairs of initially flat wafers to accumulate bow as they bond together. Thus a pair of very flat wafers can become a double thickness wafer with appreciable bow. Due to the increased thickness, this becomes a problem. Use of steel chucks during alignment and contacting, and wafer shape measurement before and after bonding were found to be effective at removing this.

Other factors that were investigated, include the surface roughening effect of buffered oxide etches used to remove “hard masks” after the DRIE steps. These were found to increase roughness to unacceptable levels after prolonged exposures, but were not usually a problem.

The influence of chemical mechanical polishing was investigated [8]. For standard silicon wafers this was found to have negligible influence on surface quality.

Particles were found to be a routine source of bond failures which could be avoided by rigidly following clean room protocols.

As a result of the study and associated experiments bonding was transformed to be a very robust step in the microengine fabrication process sequence.

4.0 PROCESSES USED TO CREATE SILICON CARBIDE IN HYBRID STRUCTURES

As described in the first lecture of this two-lecture series, the structural design of the microengine requires the use of silicon/silicon carbide hybrid structures. This is shown schematically in figure 20. The rationale behind this feature is that the silicon carbide provides significant structural reinforcement, while permitting most of the critical tolerances to be achieved in silicon, using the well-established microfabrication processes.

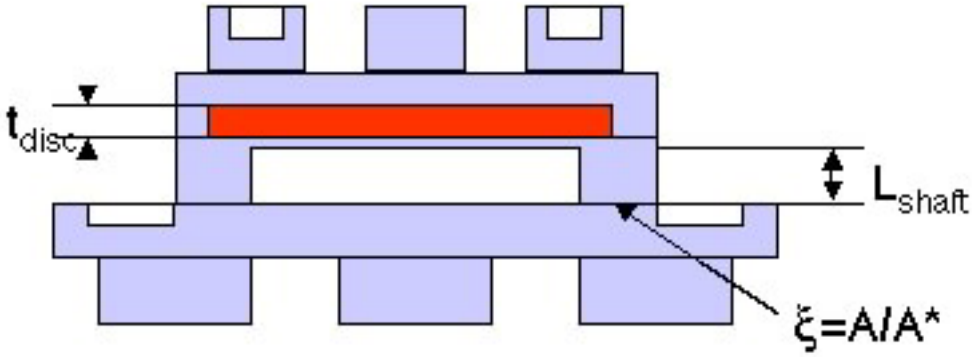


Figure 20: Schematic of Hybrid Structure Concept in which a Silicon Spool is Reinforced with Silicon Carbide.

The key process steps are shown in figure 21. They are aligned etching, chemical vapour deposition of SiC, planarization of the Si/SiC surfaces and bonding of the hybrid wafer surface to another Si wafer. Deep etching of silicon is well-understood and required little process development. Each of the other three key processes will be discussed in turn.

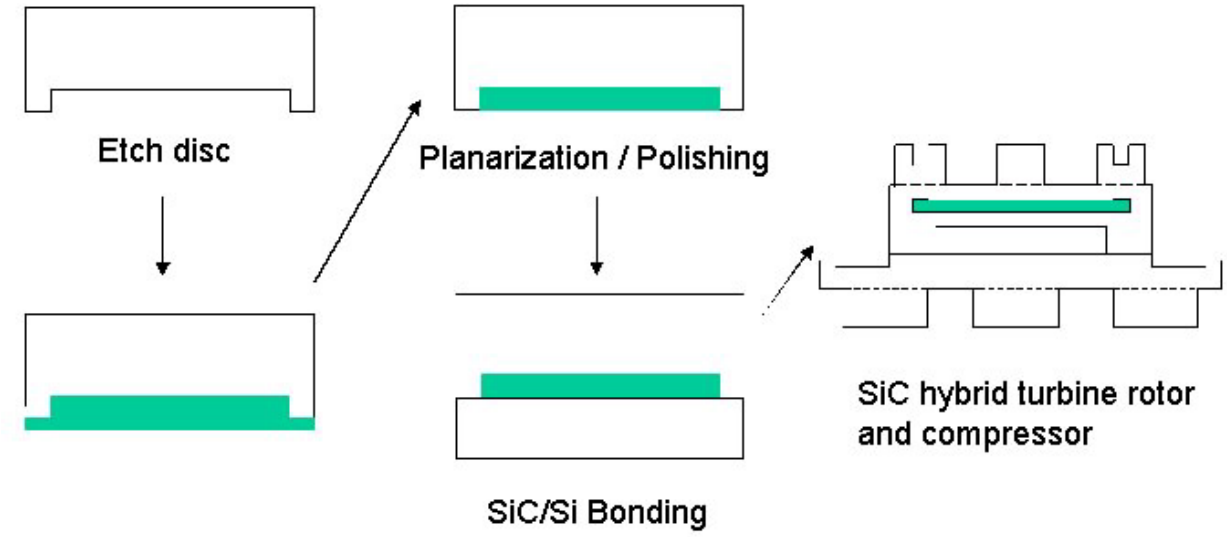


Figure 21: Schematic Process Flow for Creation of a Si/SiC Hybrid Spool.

4.1 Chemical Vapour Deposition of SiC

The key requirement for the SiC deposition is that it is deposited with very low levels of residual stress. The presence of residual stress causes wafer curvature which makes subsequent processes very difficult. A comprehensive study of the origins of residual stress in SiC has been conducted and can be found elsewhere [10]. SiC is deposited from a methyl-trichlorosilane precursor with a hydrogen carrier gas. Deposition occurs at low pressure and temperatures in excess of 1000°C. The deposited material has a highly columnar grain structure, as shown in figure 22. In addition there are multiple stacking faults visible within the grains. The columnar microstructure and the presence of stacking faults leads to the potential for high levels of residual stress.

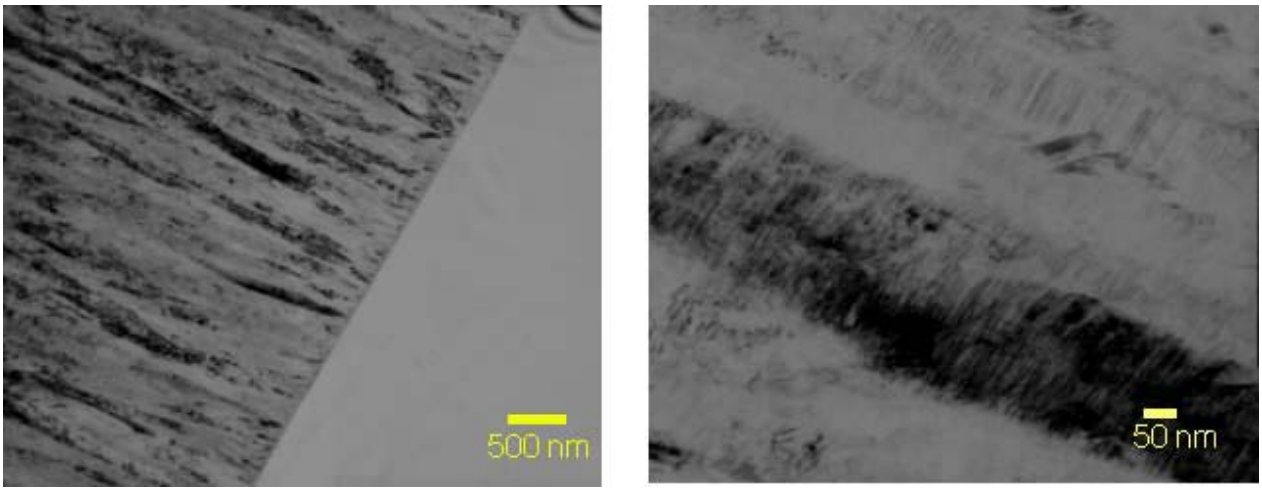


Figure 22: Transmission Electron Micrographs of SiC Grains on an Si Substrate.

The residual stress can be decoupled into two components: the thermal component (due to thermal expansion mismatch) and the "intrinsic" component due to the microstructure and growth processes. Wafer curvature measurements were used to characterize the residual stress as a function of deposition conditions. Independent measurements and accompanying analysis were used to separate the intrinsic and thermal components. Data was obtained as a function of process conditions and these are shown in figure 23 and 24. As can be seen it is possible to control the process conditions to achieve near zero residual stress. This has proved to be a very robust process, with in excess of fifty wafers being successfully processed to date.

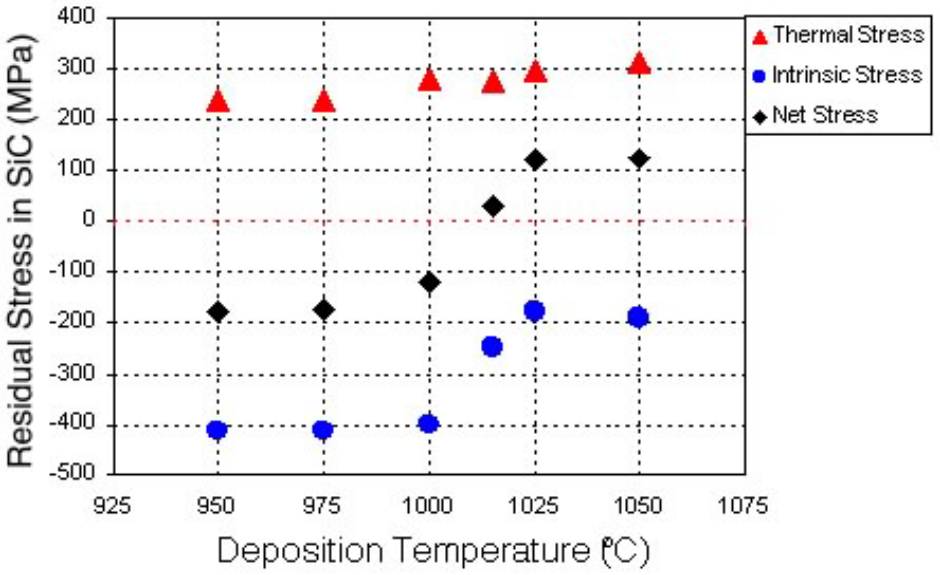


Figure 23: Variation of Residual Stress with Deposition Temperature for CVD SiC.

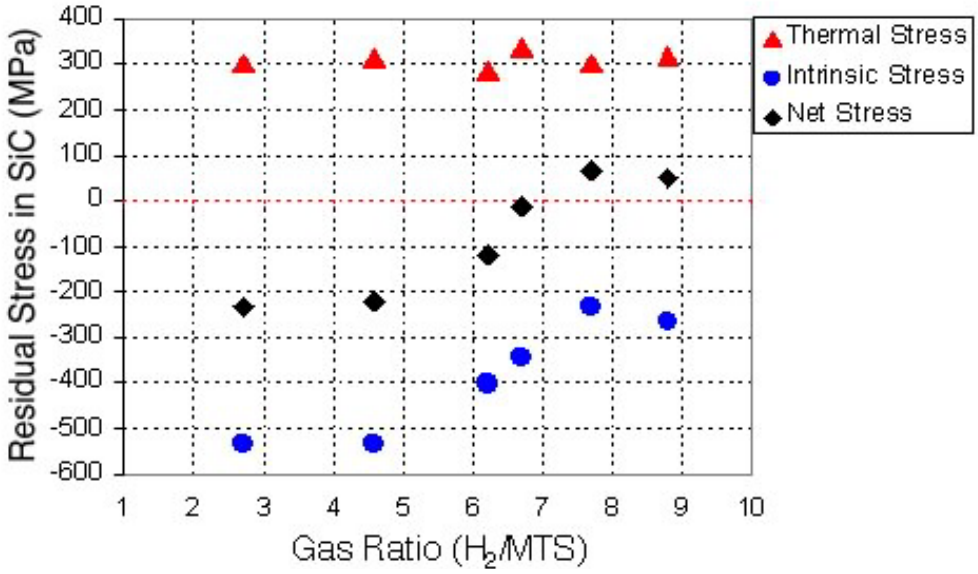


Figure 24: Variation of Residual Stress with Gas Ratio for CVD SiC.

4.2 Planarization of Si/SiC Hybrid Structures

A conventional diamond polishing procedure has been used to generate smooth Si/SiC surfaces. A polished wafer is shown in figure 25. The SiC reinforcing disks are clearly visible.

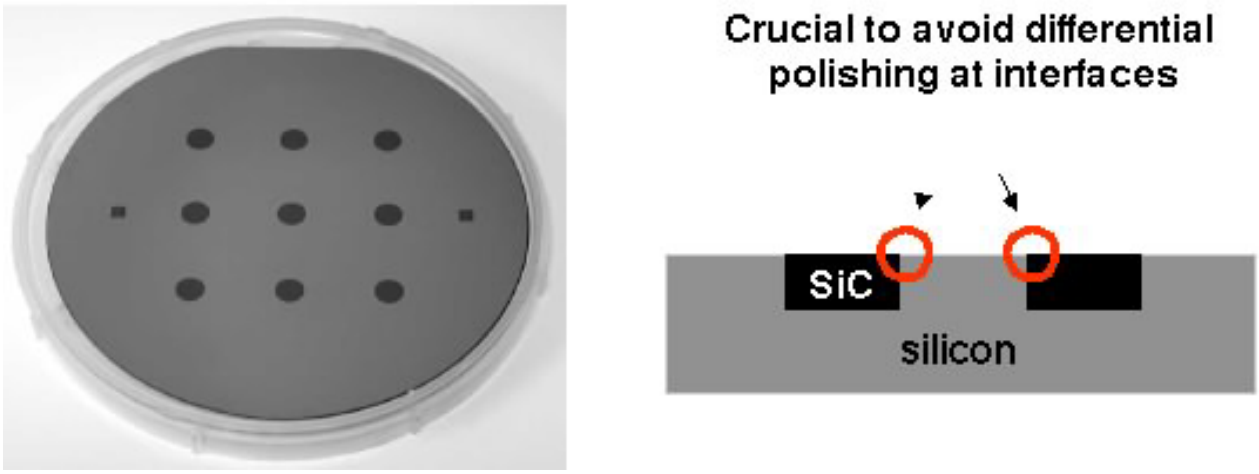


Figure 25: Polished Si/SiC Hybrid Wafer.

This process is still not sufficiently robust. Problems encountered include fracture of the wafers during polishing and the presence of height variations due to the hardness difference between the Si and SiC areas. Nevertheless progress has been made and some sufficiently smoother wafers have been generated suitable for bonding.

4.3 Bonding of Si/SiC Hybrid Wafers

Initial attempts at bonding utilized identical procedures as for bonding pairs of Si wafers (see section 3). However, the inadequacies of the polishing process and the occasional appearance of SiC nodules on the surfaces meant that this did not yield successful bonds. The process was modified by the inclusion of the deposition of a moderately thick layer of silicon oxide. The oxide layer overcoats any height variations in the Si/SiC layer. It is readily planarized by CMP to yield a bondable interface. A cross-sectional micrograph of the resulting composite interface is shown in figure 26.

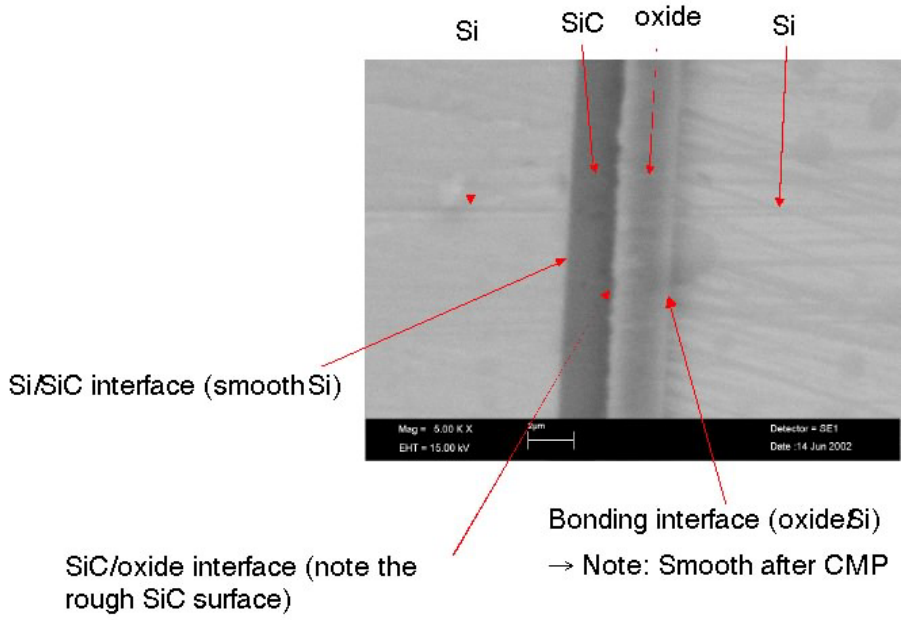


Figure 26: Cross-Section SEM of Si/SiC/SiO_2/Si Interface Layers.

Mechanical testing has been conducted which reveals that the silicon oxide layer is sufficiently thin that it has little effect on the structural integrity of the interface, at room temperature and at high temperature. Further work is required to refine this process so that high process yields are achieved, however, it appears to be highly feasible.

5.0 SUMMARY

This lecture has provided an overview of three key process issues addressed as part of the MIT microengine project. Key concepts covered have been:

1) Highly controlled deep reactive ion etching. An extensive design of experiments approach was utilized to achieve the required process control, for parallelism, uniformity and surface quality.
2) High quality wafer bonding. A mechanics framework has been developed that has allowed for high process yields out of the direct wafer bonding process to be achieved.
3) Fabrication of Si/SiC hybrid structures. Critical process steps are: residual stress control in CVD SiC deposition, planarization of Si/SiC hybrid surfaces and bonding of Si/SiC surfaces, utilizing silicon oxide interlayers.

Readers of these lecture notes interested in more details should follow up the references or contact the author.

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